



12-20-01

Docket No. MIT7759DIVCON

A

NEW APPLICATION TRANSMITTAL12/17/01  
10/002689 PRO

Transmitted herewith for filing is the patent application of:

Inventor(s): Eugene A. Fitzgerald

For (title): CONTROLLING THREADING DISLOCATION DENSITIES IN Ge  
ON Si USING GRADED GeSi LAYERS AND PLANARIZATION1. **Type of Application**

- Utility  
 Design

2. **Small Entity**

- Yes  
 No

3. **Benefit of Prior U.S. Application(s) Under 35 U.S.C. §120**

This application is a:

- Divisional  
 Continuation  
 Continuing Patent Application (CPA) under 37 C.F.R. §1.53(d)  
 Continuation-in-part (CIP),

and hereby claims benefit under 35 U.S.C. §120 to the following applications:

SERIAL NUMBER	FILING DATE
09/712,605	11/14/00

4. **Benefit of Non-U.S. Application Under 35 U.S.C. §119(a)-(d)**

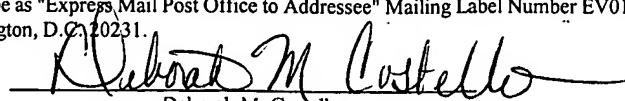
This application claims priority under 35 U.S.C. §119(a)-(d) to the following foreign application(s) and/or inventor certificate(s):

COUNTRY	APPLN. NUMBER	FILING DATE
None		

Certified copy(ies) of the application(s) and/or inventor certificate's from which priority is claimed:

- is(are) attached;  
 will follow.

I hereby certify that this New Application Transmittal and the documents referred to as enclosed therein are being deposited with the United States Postal Service on December 17, 2001 in an envelope as "Express Mail Post Office to Addressee" Mailing Label Number EV016162108US addressed to the: Assistant Commissioner of Patents, Washington, D.C. 20231.

  
Deborah M. CostelloCERTIFICATE OF EXPRESS MAIL UNDER 37 C.F.R. §1.10

I hereby certify that this New Application Transmittal and the documents referred to as enclosed therein are being deposited with the United States Postal Service on December 17, 2001 in an envelope as "Express Mail Post Office to Addressee" Mailing Label Number EV016162108US addressed to the: Assistant Commissioner of Patents, Washington, D.C. 20231.

5. **Benefit of Provisional Application Under 35 U.S.C. §119(e)**

This application claims priority to the following provisional application(s):

SERIAL NUMBER	FILING DATE

6. **Papers Enclosed Which Are Required For Filing Date Under 37 C.F.R. §1.53**

21 Pages of Specification, including claims, abstract & coversheet

5 Sheets of Drawing

7. **Additional Papers Enclosed**

- Copy of Declaration and Power of Attorney as filed in parent
- Preliminary Amendment
- Information Disclosure Statement (37 CFR 1.98) and Form PTO-1449
- Copy of Assignment and Form PTO-1595 as filed in parent
- Petition and Fee For Extension of Time
- Preliminary Amendment, clean copy of claims as amended and clean copy of amended page 1 of specification
- Other \_\_\_\_\_

8. **Application Filing Fee Calculation**

- A.  Utility Application

FEE CALCULATION:

Total Claims: 34 - 20 = 14 × \$18 = \$252.00

Independent Claims: 4 - 3 = 1 × \$84 = \$84.00

Basic Fee: .....\$740.00

Multiple-Dependent-Claim Fee : .....\$

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Total of the Above Calculations: ..... \$1,076.00

- Amendment canceling extra claims enclosed.
- Amendment deleting multiple dependencies enclosed.
- Fee for extra claims is not being paid at this time.

B.  Design application - \$320 \$

Application Filing Fee Sub-Total ..... \$

C.  Less 50% reduction for small entity..... \$

D.  Non-English Specification - \$130..... \$

**TOTAL FILING FEE ..... \$1,076.00**

## 9. Payment

- Enclosed

Check in the amount of the Total Filing Fee set forth above.

Charge Account No. 19-0079 in the amount of Total Filing Fee set forth above. A duplicate of this transmittal is attached.

Not Enclosed

The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§1.16 and 1.17 that may be required by this paper or any paper filed in connection with this Patent Application, or refund any overpayment to our Deposit Order Account No. 19-0079.

Respectfully submitted,

Matthew Edmonson

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**CONTROLLING THREADING DISLOCATION DENSITIES IN Ge ON Si USING  
GRADED GeSi LAYERS AND PLANARIZATION**

J1010 U.S. PRO  
10/022689  
12/17/01



**PRIORITY INFORMATION**

This application is a continuation of Ser. No. 09/712,604 filed on November 14, 2000 which is a continuation of 09/265,016 filed March 3, 1999, which is a divisional of Ser. No. 09/103,672 filed June 23, 1998, which claims priority from provisional applications Ser. No. 60/050,602 filed June 24, 1997 and 60/059,765 filed September 16, 1997.

**BACKGROUND OF THE INVENTION**

The invention relates to a method of creating flat, crack-free low-dislocation-density mismatched semiconductor layers, and of controlling threading dislocation densities in Ge on Si using graded SiGe layers.

The progression of electronic and optoelectronic components and systems is creating a need for more complex system-level functions to be incorporated at the chip level. One of the effects of this demand is to bring ever-increasing pressure to use materials that are not lattice-matched to common substrates.

The technological significance of a totally miscible GeSi system has been well documented. In particular, relaxed graded GeSi buffers have been used as "substrates" for the growth of high electron mobility structures and for the integration of III-V devices on Si. The relaxed graded buffer introduces a 4% lattice mismatch between Si and Ge gradually, resulting in a disperse, three-dimensional misfit dislocation network. Strain-relieving glide of threading dislocations is facilitated, preventing the accumulation of mismatch strain. Because threading dislocations present in the initial layers can also be used to relieve strain in subsequent layers, the nucleation of additional dislocations is suppressed as the graded layer growth progresses.